HIGH SPEED LOW POWER FULL ADDER FOR ARITHMATIC OPERATION WITH GDI TECHNIQUE

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Abstract - This paper presents to high speed and low power CMOS full adder cells. The full adder cells are utilization to low power by using XOR and XNOR gate architectures with pass transistor logic and transmission gate. All simulation results have been carried out by using EDA Tool Tanner simulator based on 180 nm CMOS technology . In comparison with other 1 bit adder cells, simulation results show that have used low power consumption and power delay product of SUM and C_{OUT}. Gate diffusion input (GDI) a new technique allow reducing power consumption, Propogation delay, area of digital circuit while maintaining low complexity of logic design. implementing 8 bit parallel adders *like RCA adder* as an application.

Index Terms - gate diffusion input, pass transistor logic, transmission gates, CMOS, parallel adder, ripple carry adder, very high speed hardware description language.

1. INTRODUCTION

Energy efficiency is one of the most required features for modern electronic system design for high performance and portable application in one hand, the ever increasing market segment of portable electronic device demands the availability of low power building blocks that enable the implementation of long lasting battery operated systems. On the other hand, the general trend of increasing operating frequencies and circuit complexity, in order to cope with the throughput needed in modern high-performance processing applications, requires the design of very high-speed circuits.

Addition is a fundamental arithmetic operation that is broadly used in many VLSI systems, such as application-specific digital signal processing (DSP) architectures and microprocessors. This module is the core of many arithmetic operations such as addition, subtraction, multiplication, division and address generation. As stated above, the full-adder would affect the system's overall performance. Thus, taking this fact into consideration, the design of a full-adder having low-power consumption results of great interest for the implementation of modern digital systems.

In this paper, we design full adder systems are considered performance of circuits, number of transistor, speed of circuit, chip area, threshold loss and full swing output and the most devices such as cell phone, laptop computer, tablet etc. that need a low power and high speed for components are requirements. For this reason, design of low power is the research problems. In the paper is proposed full adder base on 180 nm CMOS technology which operation for low supply voltage at 5V.

2. LITERATURE REVIEW :

2.1 Literature Survey :

There are different design techniques to implement a digital logic circuit. In this regard many innovative designs for basic logic functions have appeared in the literature recently. This includes static CMOS, mirror image, CMOS transmission gates, pass transistor logic circuits: CPL and DPL.

Static CMOS circuits are based on duality principle in which p-block is obtained as the dual network of the n-block. Output is connected to ground through n-block and to V_{DD} through dual p-block. In mirror image circuits, p-block is exactly mirror image of n-block which leads to a fully symmetric circuit topology and hence easy to design. CMOS transmission gates also known as CMOS pass gates consist of one pMOS and nMOS transistor, connected in parallel and complementary signals are applied to gate of both transistors. This transmission gate works as a bidirectional switch. The complexity of CMOS pass gate logics can be reduced by adopting CPL. It consists of purely nMOS transistors for logic operations. All inputs are applied in complementary form and output is also obtained in complementary form. The elimination of pMOS transistors gives rise to threshold voltage drop whenever high signal is passed from the nMOS. DPL is modified version of CPL for low voltage

applications. Instead of using only nMOS both pMOS and nMOS are used. pMOS passes logic high signal whereas nMOS passes logic low signal in order to achieve full output swing. Thus, using both pMOS and nMOS reduces threshold voltage drop as well as power consumption.

The implementation of the full adders can be divided into several categories. The conventional design of 1-bit full adder circuit uses standard static CMOS and complementary pass transistor logic circuits.

In the last decade, some new designs and optimizations on full adder circuits for the deep submicron technology were reported. Based on this full adder has gone through substantial improvement in power consumption, power-delay product, speed and area. Thus, these circuits have better performance than conventional designs. Starting with the conventional 28T full adder implemented using mirror technique and then gradually moving towards full adder consisting of 9T

3. METHODOLOGY

3.1 Conventional 28T CMOS Full Adder

COUT is generated first equation. Then the sum and COUT is derived from the shown in above.

$$S = A \oplus B \oplus C_{IN} \quad (1)$$

$$C_{OUT} = (A \cdot B) + (C_{IN} \cdot (A \oplus B)) \quad (2)$$

In this implementation the final OR gate before the carry out output may be replaced by an XOR gate without altering the resulting logic. In this way COUT can be implemented as

$$C_{OUT} = (A \cdot B) \oplus (C_{IN} \cdot (A \oplus B)) \quad (3)$$

3.2 20T Transmission Gate Full Adder

It produces buffered outputs of proper polarity and carry with the disadvantage of high power consumption. In the circuit we followed by two transmission gates which Subsequently 8-T XNOR module follows.CIN and are multiplexed which can controlled or (A⊗B).Similarly the COUT can multiplexing A and CIN which is controlled by (A, B).

3.3 14T Full Adder14T Full Adder

The 14T full adder contains a 4T PTL XOR gate. This circuit which in the next stage is inverted to produce XNOR. These XOR and XNOR are used simultaneously and COUT. The signals CIN and controlled either by (A⊕B)can be calculated by multiplexing (A⊕B.)

3.4 10T Full Adder realized by GDI Structure

It requires two XOR gate one MUX. (GDI CELL) XOR gate which can be implemented by 4-transistor and MUX function can be implemented by 2-transistor.

3.5 Proposed Adder Schematic with 9T

It consist of three modules. Module 1 comprises 5T XOR-XNOR module. Module 2 and 3 are GDI 2x1 MUX with different inputs and select lines which produce carry and sum output respectively.

4. TOOLS AND PLATFORM

4.1 Software Used

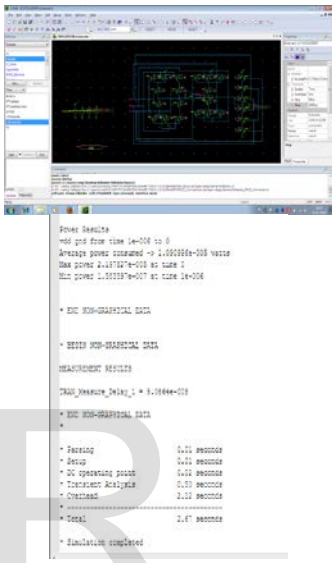
EDA tool tanner

4.2 Language Used

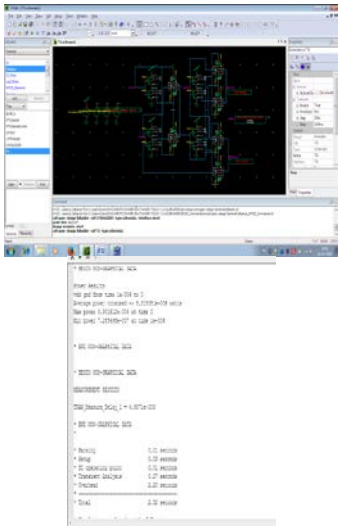
VHDL

5. RESULTS AND DISCUSSION

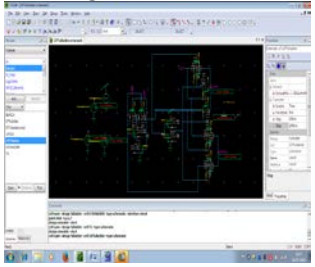
5.1 Synthesis and simulation results of 28T CMOS full adder

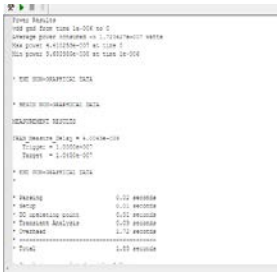


5.2 Synthesis and simulation results of 20T Transmission Gate full adder

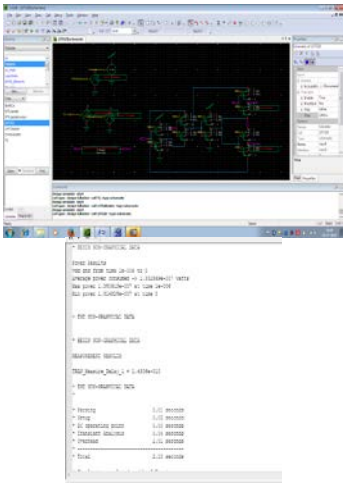


5.3 Synthesis and simulation results of 14T with Pass Transistor Logic



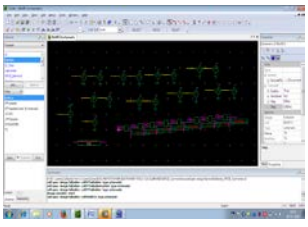


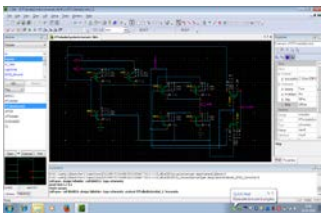
5.4 Synthesis and simulation results of 10T with GDI Cell



5.5 Synthesis and simulation results of 9T Full Adder

5.6 Synthesis and simulation results of 8 bit RCA with 9T





5.7 Comparative analysis of various type of Full Adder:

The full adder circuit is simulated using EDA tool tanner at voltage 5V using 180nm CMOS technology .The delay has been measure between the time when the changing input reaches of voltage level to the time it output reaches of voltage level for both rising and fall transition for Sum and C_{out}. The results indicate that the delay of the proposed full adder circuit is smaller than previous circuit as shown in table 1.

Table 1

Comparative analysis of various type of Full Adder

Circuit Name	Average Power (W)	Delay (s)
28T CMOS Full Adder	1.09×10^{-5} W	0.508 ns
20T Transmission gate full adder	5.31×10^{-6} W	0.498 ns
14 Transistors with pass transistor logic	1.7204×10^{-7} W	0.400 ns
10T with GDI Cell Full Adder	1.33×10^{-7} W	0.143 ns
9T Full Adder	2.5000×10^{-11} W	0.0063 ns
8-bit RCA (Ripple Carry Adder)	2.5000×10^{-11} W	0.0062 ns

6. CONCLUSION

The new implementation of mod GDI is based on the logic formulation architecture, Mod-GDI gates lower the transistor count and in turn the silicon area required when compared to standard static CMOS and dynamic CMOS based designs. The problem of fabrication of GDI gates in standard nano-scale CMOS technology is overcome by connecting the sources of PMOS and NMOS to VDD and GND respectively, in Mod-GDI logic style. The mod GDI cell also improves swing degradation problem, which is the major problem in basic GDI cell. VDD and GND interconnect wires are not required because the Mod-GDI cell requires VDD and GND only to supply the body or bulks. This is in contrast to the majority previous implementations, which would still need VDD and GND to perform the operation. The comparison between our analysis and prior works shows that the mod GDI is one of this logic styles for low power digital design does provide many advantages. In short, the proposed Mod-GDI logic style based designs can be taken a better alternative in future.

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